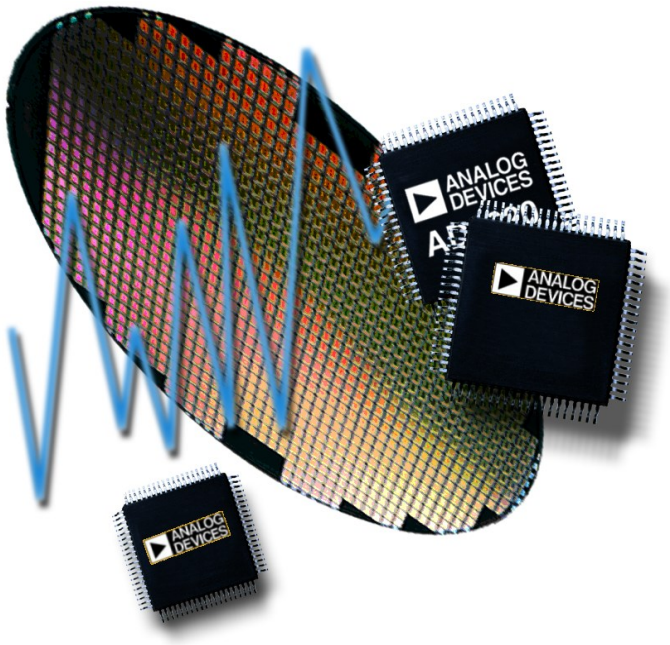

Reliability Report

Report Title: LTM4673 Material Set Change Qualification

Report Number: 22615

Revision: A

Date: 1 September 2024

Summary

This report documents the successful completion of the reliability qualification requirements for the release of the material set change of the LTM4673 product in a 361-CSP_BGA package. The LTM4673 is Quad Output µModule Regulator with Digital Power System Management. The only change made is the die thickness from 450um to 200um.

Die/Fab Product Characteristics

Table 1: Die/Fab Product Characteristics

Product Characteristics	Product(s) to be qualified	
Generic/Root Part #	LTM4673	LTM4673
Die Id	3636	7150
Die Size (mm)	2.29 x 3.35	2.54 x 5.08
Wafer Fabrication Site	TSMC	TSMC
Wafer Fabrication Process	0.35um BCDMOS	0.35um BCDMOS
Die Substrate	Si	Si
Metallization / # Layers	AlCu/4	AlCu/4
Polyimide	No	No
Passivation	undoped-oxide/SiN	undoped-oxide/SiN

Die/Fab Test Results

Table 2: Die/Fab Test Results - 0.35um BCDMOS at TSMC

Test Name	Specification	Conditions	Device	Lot #	Fail/SS
High Temperature Storage Life (HTSL)	JESD22-A103	150°C, 2,000 Hours	LTM4673	Q16998.1HTS	0/45
				Q16998.3HTS	0/45
				Q16998.5.HTS	0/45
Highly Accelerated Temperature and Humidity Stress Test (HAST)[1]	JESD22-A110	110C 85%RH 17.7 psia, Biased, 264 Hours	LTM4673	Q16998.3.BHAST	0/25
				Q16998.BHAST	0/25
				Q16998.BHAST3	0/25
High Temperature Operating Life (HTOL)	JESD22-A108	Ta = 125C, Biased, 1000 hours	LTM4673	Q16998.1HTOL	0/77
				Q16998.2HTOL	0/77
				Q16998.3HTOL	0/77
Power Cycle	JESD22-A122	Tj=25°C to 80°C, Biased, 50,000 Cycles.	LTM4673	1042723.1	0/8
				1048448.1	0/8
				1073551.1	0/8

[1] These samples were subjected to preconditioning (per J-STD-020 Level 3) prior to the start of the stress test. Level 3 preconditioning consists of the following: Bake: 48 hrs @ 125°C, Unbiased Soak: 192 hrs @ 30°C, 60%RH, Reflow: 3 passes through an oven with a peak temperature of 245°C.

Package/Assembly Product Characteristics

Table 3: Package/Assembly Product Characteristics - 361-CSP_BGA at ASE Korea

Product Characteristics	Product(s) to be qualified
Generic/Root Part #	LTM4673
Package	361-CSP_BGA
Body Size (mm)	16.00 x 16.00 x 4.72
Assembly Location	ASE Korea
MSL/Peak Reflow Temperature(°C)	4 / 245°C
Mold Compound	Sumitomo G311E
Substrate Material	BT Resin
Solder Ball Composition	96.5_Sn3_Ag0.5Cu
Solder Ball Size (mm)	0.50

Package/Assembly Test Results

Table 4: Package/Assembly Test Results - CSP_BGA at ASE Korea

Test Name	Spec	Conditions	Generic/Root Part #	Lot #	Fail/SS
Solder Heat Resistance (SHR)	J-STD-020	MSL-4	LTM4673	Q22615.1.MSL4[3]	0/231
Temperature Cycling (TC)[2]	JESD22-A104	-55°C/+125°C, 1,000 Cycles	LTM4673	Q22615.1.TC[3]	0/77
Temperature Cycling (TC)[1]	JESD22-A104	-55°C/+125°C, 1,000 Cycles	LTM4673	Q16998.3TC	0/77
				Q16998.4.TC	0/77
				Q16998.TC3	0/77
Highly Accelerated Temperature and Humidity Stress Test (HAST)[1]	JESD22-A110	110C 85%RH 17.7 psia, Biased, 264 Hours	LTM4673	Q16998.3.BHAST	0/25
				Q16998.BHAST	0/25
				Q16998.BHAST3	0/25
Unbiased HAST (UHAST)[1]	JESD22-A118	110C 85%RH 17.7 psia, 264 Hours	LTM4673	Q16998.3UHAST	0/77
				Q16998.7.UHAST	0/77
				Q16998.UHAST3	0/77

[1] These samples were subjected to preconditioning (per J-STD-020 Level 3) prior to the start of the stress test. Level 3 preconditioning consists of the following: Bake: 48 hrs @ 125°C, Unbiased Soak: 192 hrs @ 30°C, 60%RH, Reflow: 3 passes through an oven with a peak temperature of 245°C.

[2] These samples were subjected to preconditioning (per J-STD-020 Level 4) prior to the start of the stress test. Level 4 preconditioning consists of the following: Bake: 48 hrs @ 125°C, Unbiased Soak: 96 hrs @ 30°C, 60%RH, Reflow: 3 passes through an oven with a peak temperature of 245°C.

[3] Stress test with 200µm die.

Note: J-STD-020 rework compatibility was verified passing by performing Bake: 48 hrs @ 125°C, Unbiased Soak: 8 hrs @ 30°C, 60%RH, Reflow: 1 pass through a reflow oven with a peak temperature of 260°C.

ESD and Latch-Up Test Results

Table 5: ESD Test Results

ESD Model	Generic/Root Part #	Package	ESD Test Spec	ESD Test Spec	Highest Pass Level	First Fail Level	Class
FICDM	LTM4673	361-CSP_BGA	JS-002	1Ω, Cpkg	±750V	±1000V	C2b
HBM	LTM4673	361-CSP_BGA	JESD22-A114	1.5kΩ, 100pF	±3500V	±4000V	2

Table 6: Latch Up Test Result

LU Test Spec	Generic/Root Part #	Passing Current	Passing Over-Voltage	Temperature (T_A)	Class
JESD78	LTM4673[1]	+200mA, -200mA	+16V, 4.6V,3.975V	25°C	I

[1] Stress test with 200µm die.

Approvals

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